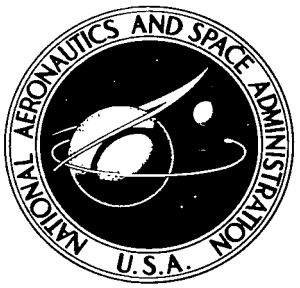
NASA TECHNICAL NOTE

NASA TN D-4176






NASA TN D-4176

# STATIC PARASITIC SPEED CONTROLLER FOR BRAYTON-CYCLE TURBOALTERNATOR

*by John L. Word, Raymond L. E. Fischer, and Bill D. Ingle*

*Lewis Research Center*

*Cleveland, Ohio*

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • SEPTEMBER 1967

NASA TN D-4176

# STATIC PARASITIC SPEED CONTROLLER FOR BRAYTON-CYCLE TURBOALTERNATOR

By John L. Word, Raymond L. E. Fischer, and Bill D. Ingle

Lewis Research Center
Cleveland, Ohio

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

For sale by the Clearinghouse for Federal Scientific and Technical Information
Springfield, Virginia 22151 – CFSTI price $3.00

# STATIC PARASITIC SPEED CONTROLLER FOR BRAYTON-CYCLE TURBOALTERNATOR

by John L. Word, Raymond L. E. Fischer, and Bill D. Ingle

Lewis Research Center

## SUMMARY

A static parasitic loading speed-controller design is presented with supporting experimental data obtained from a breadboard model. The speed controller was designed to be used with the turboalternator in a 400-hertz Brayton-cycle energy-conversion system.

The speed controller consists of three separate channels, each of which senses frequency from separate phases of the turboalternator and controls the power to a three-phase parasitic load. Each channel comprises a frequency discriminator, a magnetic preamplifier, and three output stages consisting of silicon-controlled rectifiers and their magnetic firing circuits. The power dissipated in the parasitic load is determined by phase control of the multiple silicon-controlled-rectifier output stages. An overspeed subcircuit ensures that full parasitic power will be maintained should an overspeed condition occur.

The speed controller is designed to operate normally from 50 to 200 percent of rated speed and from 50 to 140 percent of rated voltage. Using silicon-controlled rectifiers as the power handling devices enables low shutoff losses to be obtained.

## INTRODUCTION

In a turbine drive system, a constant operating speed can be obtained only when the input power equals the output power, including losses. In a turboalternator electrical power-generating system, where a constant operating speed is required, a speed controller must be utilized to maintain a proper balance between input and output.

Basically, there are two types of speed controllers: those which control the turboalternator input power by adjusting the flow of gas, and those which control the turboalternator output power by adjusting the load on the turboalternator. Controllers of the

latter type are referred to in this report as parasitic speed controllers and may consist of a tandem generator, a brake, or a resistance load.

All the previously mentioned speed controllers employ moving parts, except for the resistive-loading parasitic speed controller. The static resistive-loading parasitic speed controller was selected for this application to avoid the problems that are associated with moving parts, such as bearings and seals.

A program was initiated to design, build, and evaluate a speed controller of this type for use with the turboalternator in a 400-hertz Brayton-cycle energy-conversion system. The design of this speed controller and the results of an experimental evaluation are presented herein.

Resistive-loading parasitic speed controllers have been previously designed for the SNAP-2, SNAP-8, and Sunflower space power systems (refs. 1 to 3). The speed-controller design described herein retains the desirable features of these speed controllers, such as the use of multiple loads in SNAP-2. However, additional features were included in this design to make the speed controller insensitive to changes in line voltage and to obtain low shutoff losses. The speed controller employs three frequency-sensing stages, each of which drives a three-phase parasitic load. The frequency-sensing stages are so adjusted that the parasitic loads are applied in succession.

A review of the design objectives and subcircuit evaluations is presented in this report with supporting experimental data obtained from a breadboard model.

## SYMBOLS

| | |
|---|---|
| $B_{max}$ | flux density in saturation region |
| $I_1$ | output from discriminator; input to preamplifier |
| $I_2$ | output from preamplifier; input to output subcircuit |
| $I_3$ | output from amplifier; input to output subcircuit |
| $V_{LL}$ | line to line voltage |
| $V_{LN}$ | line to neutral voltage |
| $\theta_c$ | conduction angle, deg |

## DESIGN OBJECTIVES

The performance requirements of the Brayton-cycle energy-conversion system were used as a basis for determining the design objectives of the speed controller. Table I

TABLE I. - SOLAR BRAYTON-CYCLE

SYSTEM ELECTRICAL PARAMETERS

| | |
|---|---|
| Rated voltage, volts | |
| Line to line | 208 |
| Line to neutral | 120 |
| Maximum transit voltage, percent of rated voltage | 136 |
| Rated frequency, Hz | 400 |
| Steady-state frequency regulation, percent | ±1 |
| Number of phases | 3 |
| Rated lagging power factor | 0.8 |
| Maximum output power capability, kW | 10 |
| Maximum alternator input power during system startup[a], kW | 18 |

[a]See ref. 4.

TABLE II. - DESIRED SPEED-CONTROLLER

PERFORMANCE CHARACTERISTICS

| | |
|---|---|
| Maximum parasitic load power, per unit | 1.8 |
| Frequency, Hz | |
| Rated | 400 |
| Active control range | 400 to 406 |
| Normal operating range of speed controller | 200 to 800 |
| Voltage, volts (line to neutral) | |
| Rated | 120 |
| Range of insensitivity to changes in line voltages | 60 to 170 |
| Losses | |
| Shutoff | Minimum[a] |
| Full-on | Minimum[b] |

[a]To improve system efficiency.

[b]To reduce system cooling requirements.

summarizes the system parameters.

As table I indicated, the Brayton-cycle system is capable of delivering up to 10 kilowatts. Throughout this report, parasitic load power is expressed on a per unit basis in which the output power is normalized to a base of 10 kilowatts.

Table II and figure 1 summarize the desired speed-controller performance characteristics. The maximum speed-controller output power capability is 1.8 per unit, as required by the system during startup (see ref. 4).

When power is being dissipated in the parasitic load, the useful power available to the system load is reduced accordingly. Therefore, the parasitic load power must be fully shut off at 400 hertz to maximize system efficiency at rated operating conditions. The active control range of the speed controller was selected to be 400 to 406 hertz; that is, 1.8-per-unit parasitic power is applied in a 6-hertz interval starting at 400 hertz (fig. 1). This control range satisfies the steady-state frequency regulation requirement of ±1 percent since 1 per-unit parasitic power or more is applied in a 4-hertz interval (1 percent of 400 Hz), if the speed controller applies parasitic load power linearly.

The frequency and voltage ranges of the speed controller, as indicated previously, were selected to match or exceed those of the turboalternator for any conceivable transient or startup condition.

## SUBCIRCUIT EVALUATION

Figure 2 is a block diagram of the speed controller selected to satisfy the design objectives given in table II and figure 1. The speed controller has three channels, each consisting of a frequency sensing stage, a preamplifier, and three output stages. Each channel senses frequency from one phase of the alternator and controls the power to a three-phase parasitic load.

The power dissipated in the parasitic load is determined by phase control of the multiple silicon-controlled-rectifier (SCR) output stages. The use of phase-controlled switching devices in the power output stages generates harmonics in the alternator output voltage. However, the use of multiple parasitic loads could reduce the magnitude of the harmonics as compared to a single three-phase parasitic load system. The actual number of multiple parasitic loads used is a compromise between circuit complexity and the diminishing effect that each additional load has on harmonic reduction. Therefore, three multiple parasitic loads were selected with one channel per load.

After the preliminary design of the speed controller was completed, a breadboard of each subcircuit was built at the Lewis Research Center to verify and evaluate the design. The breadboards were operated at full voltage ($V_{LN}$ = 120 volts). For convenience, the output subcircuit was operated at a reduced power level of 100 watts per

load resistor. An electronic variable-frequency power supply was utilized to obtain the subcircuit characteristics.

The discussion which follows includes a description, a circuit diagram, and an experimental characteristic graph for each subcircuit. For convenience, the various direct currents are numbered on both the circuit diagrams and the graphs of subcircuit characteristics.

## Sensing Subcircuit (Discriminator)

The sensing subcircuit of a speed controller generates an output as a function of frequency. A double-tuned inductor-capacitor frequency discriminator, hereinafter referred to as the discriminator, was selected for this speed-controller design because of its high gain and fast response.

Figure 3 is a circuit diagram of the discriminator. To ensure operation over the range $V_{LN}$ = 60 to 170 volts, the secondary voltage of the input transformer $T_1$ is clipped by Zener diodes $Z_1$ to $Z_4$, thus providing a regulated voltage for the discriminator. The discriminator operates from the fundamental component of the clipped sine wave since the inductor-capacitor tuned circuits filter out the higher harmonics. Inductor $L_3$, in series with the primary winding of the transformer, is used to filter the line voltage should distortion occur because of the switching devices in the output subcircuits. Capacitor $C_3$ and inductor $L_4$ provide a filter for the output current. Further information on the operation and design of frequency discriminators is supplied in references 5 and 6.

The discriminator characteristic obtained experimentally is given in figure 4. The frequency at which the characteristic curve crosses the zero axis, referred to as the crossover frequency, is shown to be approximately 395 hertz and can be adjusted by varying the values of the capacitors $C_1$ and $C_2$. The active control range, indicated on the curve, is the range over which the parasitic load power goes from zero to its maximum value. The discriminator output current $I_1$ must be approximately 6 milliamperes or greater to maintain maximum output power. The range over which the discriminator can maintain maximum output power is indicated in figure 4.

The discriminators for phases A, B, and C are identical except for the values of capacitors $C_1$ and $C_2$. Different capacitances are used so that each discriminator will have a different crossover frequency. The crossover frequencies are sequenced approximately 2 hertz apart to make the speed controller go from no parasitic power to maximum parasitic power (1.8 per unit) in 6 hertz.

## Amplification Subcircuit (Preamplifier)

Amplification is required between the discriminator and output subcircuits. Although both magnetic and semiconductor amplifiers were investigated, a magnetic amplifier (dc to dc), referred to as the preamplifier, was selected because its circuitry involved fewer components.

Figure 5 is a circuit diagram of the preamplifier. Zener diodes $Z_{10}$ and $Z_{11}$ clip the secondary voltage of the input transformer, and thus regulate the input voltage and enable the preamplifier to operate down to $V_{LN} = 60$ volts. The two half-wave magnetic amplifiers are connected in a full-wave, rectified-output configuration, and inductor $L_{10}$ filters the output current.

A discontinuity or abrupt change in the amplifier characteristic can occur as a result of the phenomenon known as snap. Figure 6 illustrates a typical magnetic amplifier characteristic both with and without snap. References 7 to 9 give further information on the theory and design of magnetic amplifiers, including the phenomenon of snap.

A degenerative circuit utilizing a resistor network $R_{11}$ and a separate winding on the magnetic cores $M_{10}$ and $M_{11}$ was used to eliminate snap from the preamplifier. The flux set up by the induced current in the degenerative circuit is in such a direction that it opposes the change in flux that occurs during snap.

The preamplifier characteristic, obtained experimentally, is plotted in figure 7. As the input current $I_1$ is increased to 6 milliamperes, the preamplifier is driven through its active control range, and the output current $I_2$ decreases. Above 6 milliamperes, the preamplifier is being overdriven and the output current increases slightly. However, if the preamplifier is overdriven far enough, a reduction in parasitic load power occurs (a phenomenon to be discussed further in the section SPEED-CONTROLLER PERFORMANCE).

## Output Subcircuit

The output subcircuit is the power handling stage and controls the flow of current through the parasitic load. Silicon-controlled rectifiers (SCR's) were selected as the power handling devices in order to obtain low shutoff losses. Each SCR is phase controlled by a half-wave magnetic firing circuit.

Figure 8 is a circuit diagram of an output circuit and parasitic resistor. Each output subcircuit consists of a pair of SCR's, including firing circuits, connected so that the parasitic load current waveform is bidirectional as illustrated in figure 9. The number of electrical degrees during which the parasitic load current flows each half cycle is referred to as the conduction angle $\theta_c$. References 10 and 11 explain the theory and

operation of SCR's, and reference 10 (pp. 41 to 43) discusses the half-wave magnetic firing circuit.

Resistors $R_{26}$ and $R_{27}$ are utilized to match the gains of the two firing circuits and thus reduce any imbalance in the parasitic load waveform. A degenerative circuit (consisting of resistor $R_{28}$ together with the associated windings on the magnetic cores $M_{20}$ and $M_{21}$) was used in conjunction with a phase-shifting network (accomplished by capacitors $C_{20}$ and $C_{21}$) to eliminate snap from the magnetic firing circuit. The winding inductance of the magnetic cores $M_{20}$ and $M_{21}$ together with the added capacitance produced a total phase shift of approximately $30^{o}$ between the SCR gate and anode voltage. As a result of the phase shift, the maximum load conduction angle that may be obtained is limited to approximately $150^{o}$. The maximum parasitic load power of 18 kilowatts is therefore based on a $150^{o}$ conduction angle.

Figure 10 is the output subcircuit characteristic obtained experimentally from a breadboard. Both conduction angle and parasitic load power are plotted as functions of the input current $I_2$. The input current $I_2$ is the direct current out of the preamplifier and has a minimum shutoff value of 6.5 milliamperes. The parasitic load power reaches its maximum value of 0.2 per unit (2 kW) per resistor at the maximum conduction angle.

## Overspeed Subcircuit

The purpose of the overspeed subcircuit is to maintain full parasitic power on the system should the line frequency exceed the useful range of the discriminator. Several overspeed subcircuits were investigated, but the subcircuit of figure 11 was selected because its circuitry involves fewer components. The overspeed subcircuit consists of a volts-per-hertz sensing circuit, a temperature-compensating circuit, a magnetic amplifier, and a direct-current bias circuit for the amplifier.

The volts-per-hertz transformer $T_{32}$ produces an output voltage the average of which is proportional to the product of the flux density in the saturation region $B_{max}$ and frequency. The flux density in the saturation region $B_{max}$ is a core parameter that varies with temperature. Therefore, at any constant temperature, the voltage from the sensing circuit is proportional to frequency.

However, if the temperature of the core increases, $B_{max}$ will decrease and thus decrease the sensing-circuit output voltage. A temperature-compensating circuit was introduced to compensate for this voltage change with temperature. The primary Zener diodes were selected to have a positive temperature coefficient so that the output of the temperature-compensation circuit would increase with temperature. Thus, as temperature increases, the increasing output voltage of transformer $T_{30}$ compensates for the decreasing output voltage of transformer $T_{32}$.

The output of the sensing circuit is compared to a voltage reference, and the difference is used to drive the amplifier. The voltage level of this reference, determined by the temperature-compensated Zener diode $Z_{34}$, determines the frequency at which the subcircuit starts to control parasitic load power. The Zener diodes across the input winding of transformer $T_{32}$ protect circuit components if excessive voltage transients occur but otherwise do not appreciably affect the performance of the circuit.

The output current of the overspeed subcircuit amplifier is fed into nine output subcircuits. The amplifier is similar to the preamplifier except that there are no provisions for reducing snap.

An overspeed subcircuit was fabricated, and the control characteristic obtained experimentally as shown in figure 12. At frequencies below the turn-on point of the subcircuit, the sensing circuit produces no significant output and the direct-current bias holds the amplifier output current $I_3$ to a minimum. At high frequencies, the current from the sensing circuit drives the amplifier to a full-on state, and maximum output current results. Indicated on the characteristic curve is the point at which the overspeed subcircuit is capable of maintaining maximum parasitic load power.

The discontinuity or abrupt change in the control characteristic, observed at the turn-on frequency, is caused by the presence of control snap in the magnetic amplifier. This snap was not eliminated since the overspeed subcircuit turns full on several hertz before the discriminator begins to lose control.

## SPEED-CONTROLLER PERFORMANCE

Additional subcircuits were fabricated and interconnected, as shown in figure 13, in order to study the performance of the speed controller. Only one output subcircuit and parasitic resistor per channel was utilized. Tests were conducted to determine the control characteristic, the time delay, the losses, and the off-design voltage performance of the speed controller.

The subcircuits were operated at $V_{LN}$ = 120 volts but with parasitic power reduced to 100 watts per resistor. (Full parasitic power was employed only when measuring losses.) The test setup for the speed controller utilized two alternating-current static variable-frequency power supplies. A high-precision single-phase power supply was utilized to drive the frequency-sensing circuits. All other subcircuits were driven from the three-phase power supply.

## Control Characteristic

The discriminators were tuned to obtain an approximately linear control characteristic over the active range as shown in figure 14. Both curves are plots of parasitic load power against frequency at a constant line voltage $V_{LN}$ of 120 volts.

In figure 14(a), the control characteristic is plotted to show the active range of the speed controller more clearly. As can be seen, the turn-on frequency is approximately 400 hertz and the full-on frequency is approximately 406 hertz, which results in a total active range of 6 hertz. As shown, the parasitic load power varies in a smooth and continuous manner from 0 to 1.8 per unit over this range.

In figure 14(b), the control characteristic is plotted from 200 to 800 hertz both with and without the overspeed subcircuit. When operated without the overspeed subcircuit, two phenomena occur that cause a reduction in parasitic load power at high frequencies. First, a small reduction in parasitic power occurs at approximately 420 hertz because the output of the discriminator, while passing through its maximum, is slightly overdriving the preamplifier. Since the speed controller at this point is delivering approximately 1.8-per-unit parasitic load, this small reduction should not adversely affect system performance. Consequently, no steps were taken to correct this situation. Second, as the line frequency is increased to approximately 475 hertz, the output of the discriminator is reduced to the point where it can no longer maintain maximum parasitic power. Consequently, the parasitic power begins to drop and is fully off at approximately 490 hertz. As can be seen, the addition of the overspeed subcircuit eliminates this second problem by maintaining maximum parasitic power output beyond 800 hertz.

## Speed-Controller Time Delay

Time delay in this report is defined to be the time required for the parasitic load voltage to reach a new steady state (within 2 percent) for a step change in input frequency.

The time delay of a speed controller should be as small as possible, without introducing system and/or speed-controller instability, so that the response time of the system will not be increased. In this speed controller, the inductors $L_4$ (fig. 3) and $L_{10}$ (fig. 5) present in the control circuits of the magnetic amplifiers account for a large portion of the time delay.

In measuring the time delay, a small change in frequency was applied to the discriminators, which allowed the speed controller to operate entirely within its active control range. The time required for the parasitic load voltage to reach a new steady state under these conditions was approximately 130 milliseconds. The speed-controller time delay was independent of frequency and frequency change as long as the subcircuits were operated entirely within their active control ranges.

## Speed-Controller Losses

The speed-controller losses were measured under conditions of no parasitic power and full parasitic power at an input voltage $V_{LN}$ of 120 volts.

Table III shows the power and volt-ampere requirements for each subcircuit under conditions of no parasitic power. The total speed-controller losses were measured at 400 hertz and found to be 179.2 watts with a power factor of 0.937. The losses did not change significantly over the range 200 to 400 hertz.

The voltage regulation circuits (in the discriminator, preamplifier, and overspeed subcircuits), which make the speed controller insensitive to changes in line voltage over the range $V_{LN}$ = 60 to 170 volts, contribute approximately 60 to 80 watts total loss. Another important source of loss is the overspeed subcircuit. As table III indicates,

TABLE III. - SPEED-CONTROLLER POWER LOSS AND VOLT-AMPERE REQUIREMENT WITH NO PARASITIC POWER

[Measured at 400 Hz and $V_{LN}$ = 120 volts.]

| Subcircuit | Power loss, W | Volt-amperes | Subcircuits used in controller | Total power, W | Total volt-amperes |
|---|---|---|---|---|---|
| Discriminator | 19.3 | 19.5 | 3 | 57.9 | 58.5 |
| Preamplifier | 10.6 | 12.0 | 3 | 31.8 | 36.0 |
| Output | 2.5 | 3.1 | 9 | 22.5 | 27.9 |
| Overspeed | 67.0 | 69.0 | 1 | 67.0 | 69.0 |
| Total[a] | | | | 179.2 | 191.4 |

[a]Speed-controller power factor = $\frac{\text{Total power}}{\text{Total volt-amperes}} = \frac{179.2}{191.4} = 0.937$.

TABLE IV. - SPEED-CONTROLLER POWER LOSS AND VOLT-AMPERE REQUIREMENT WITH FULL PARASITIC POWER (1.8 pu)

[Measured at 407 Hz and $V_{LN}$ = 120 volts.]

| Subcircuit | Power loss, W | Volt-amperes | Subcircuits used in controller | Total power, W | Total volt-amperes |
|---|---|---|---|---|---|
| Discriminator | 16.3 | 18.3 | 3 | 48.9 | 54.9 |
| Preamplifier | 8.8 | 9.1 | 3 | 26.4 | 27.3 |
| Output | 47.0 | 48.5 | 9 | 423.0 | 436.5 |
| Overspeed | 68.0 | 68.4 | 1 | 68.0 | 68.4 |
| Total[a] | | | | 566.3 | 587.1 |

[a]Speed-controller power factor = $\frac{\text{Total power}}{\text{Total volt-amperes}} = \frac{566.3}{587.1} = 0.965$

67 watts are dissipated in this subcircuit.

Table IV shows the power and volt-ampere requirements for each subcircuit under conditions of full parasitic power. The total losses at full parasitic power were measured at 407 hertz and found to be 566.3 watts with a power factor of 0.965. The full-on losses did not change significantly over the range 407 to 800 hertz. The cooling system requirements for the speed controller are determined by the full-on losses.

## Off-Design-Voltage Performance

The performance of the experimental breadboard (fig. 13) was investigated during operation at off-design voltages. The results of speed-controller operation at reduced line voltages are recorded in table V. Table V lists the turn-on and full-on frequencies observed, as well as the maximum parasitic power dissipated as the voltage $V_{LN}$ was reduced from 120 to 60 volts. As the line voltage was decreased, both the turn-on and full-on frequencies increased, and the maximum parasitic power varied in accordance with the basic equation

$$\text{power} = \frac{(\text{rms voltage})^2}{\text{resistance}} \tag{1}$$

The rms voltage in equation (1) is a function of both the line-to-neutral alternator voltage and the maximum SCR conduction angle $\theta_c$, which is a function of many variables including line-to-neutral voltage (as discussed in ref. 7). The active control range of the speed controller remained nearly constant down to $V_{LN} = 70$ volts but increased greatly as the voltage was decreased further.

TABLE V. - REDUCED-VOLTAGE PERFORMANCE

| Line-to-neutral voltage, $V_{LN}$ volts | Turn-on frequency, Hz | Full-on frequency, Hz | Active range, Hz | Maximum parasitic power per unit |
|---|---|---|---|---|
| 120 | 400.0 | 406.0 | 6.0 | 1.8 |
| 110 | 400.2 | 406.1 | 5.9 | 1.44 |
| 100 | 400.6 | 406.3 | 5.7 | 1.13 |
| 90 | 400.9 | 407.1 | 6.2 | .937 |
| 80 | 401.2 | 408.0 | 6.8 | .725 |
| 70 | 401.8 | 411.6 | 9.8 | .54 |
| 60 | 406.0 | 423.6 | 17.6 | .378 |

The speed controller was not designed to operate below $V_{LN}$ = 60 volts, since neither transient nor startup voltage are expected to occur below this value. In fact, the speed controller malfunctions at line voltages $V_{LN}$ below 50 volts, since there is insufficient voltage available to produce the preamplifier output current required to hold the SCR's and their firing circuits in an off state. Consequently, below $V_{LN}$ = 50 volts parasitic power is dissipated in accordance with equation (1) and is independent of frequency.

The speed-controller breadboard operated normally at input voltages $V_{LN}$ up to 170 volts.

## SUMMARY OF RESULTS

Based on system considerations, design goals were established for a speed controller to be used with the turboalternator in a 400-hertz Brayton-cycle energy-conversion system. The parasitic loading speed-controller design presented herein successfully satisfies all these design goals.

An experimental breadboard was built, and tests have shown that the speed controller is capable of varying parasitic load power from zero to its maximum value in a 6-hertz interval in a smooth, continuous manner.

The speed controller has a parasitic load rating of 18 kilowatts at the maximum conduction angle of 150 electrical degrees. Low shutoff losses (approx. 179.2 W) were accomplished by utilizing silicon-controlled rectifiers as the power handling devices.

The speed controller operates normally from 50 to 200 percent of rated speed and from 50 to 140 percent of rated voltage. The problem of snap in the magnetic amplifiers was overcome by the use of degenerative circuits and phase shifting networks.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, March 29, 1967,
120-27-03-42-22.

# REFERENCES


1. Dauterman, W. E.: Snap 2 Power Conversion System Topical Report No. 27. Rep. No. ER-5908 (AEC No. NAA-SR-6319), Thompson Ramo Wooldridge Inc., June 1964.
2. Nice, A. W.; and Bradley, S. L.: Snap-8 Electrical System. Paper presented at the International Conference and Exhibit on Aerospace Electro-Technology, IEEE, Phoenix, Arizona, April 19-25, 1964.
3. Lalli, V. R.: Sunflower Rotational Speed Control Topical Report. Rep. No. ER-4947, Tapco Div., Thompson Ramo Wooldridge Inc., Mar. 1963.
4. Hurrell, Herbert G.; and Thomas, Ronald L.: Control and Startup Considerations for Two-Spool Solar-Brayton Power System. NASA TM X-1270, 1966.
5. Deutsch, Sid: Theory and Design of Television Receivers. McGraw-Hill Book Co. Inc., 1951, pp. 268-283.
6. Terman, Frederick E.: Radio Engineers' Handbook. McGraw-Hill Book Co., Inc., 1943, pp. 585-588.
7. Storm, H. F.: Magnetic Amplifiers. John Wiley & Sons, Inc., 1955.
8. Attura, George M.: Magnetic Amplifier Engineering. McGraw-Hill Book Co., Inc., 1959.
9. Staff of International Telephone and Telegraph Corp.: Reference Data for Radio Engineers. Fourth ed., American Book - Stratford Press Incorporated, 1956, pp. 323-343.
10. Staff of General Electric Co.: Silicon Controlled Rectifier Manual. Second ed., General Electric Co., 1961.
11. Staff of International Rectifier Corp.: The Controlled Rectifier. Vol. 1. International Rectifier Corp., 1962.

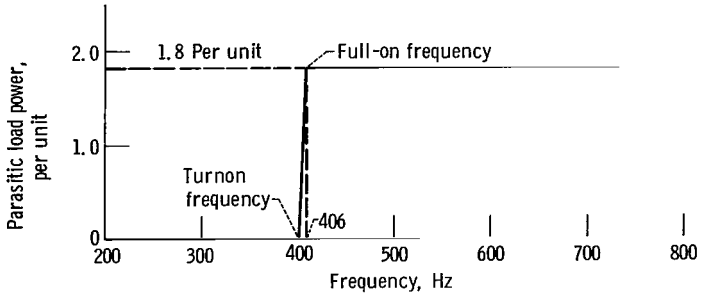



Figure 1. - Desired control characteristic of speed controller.

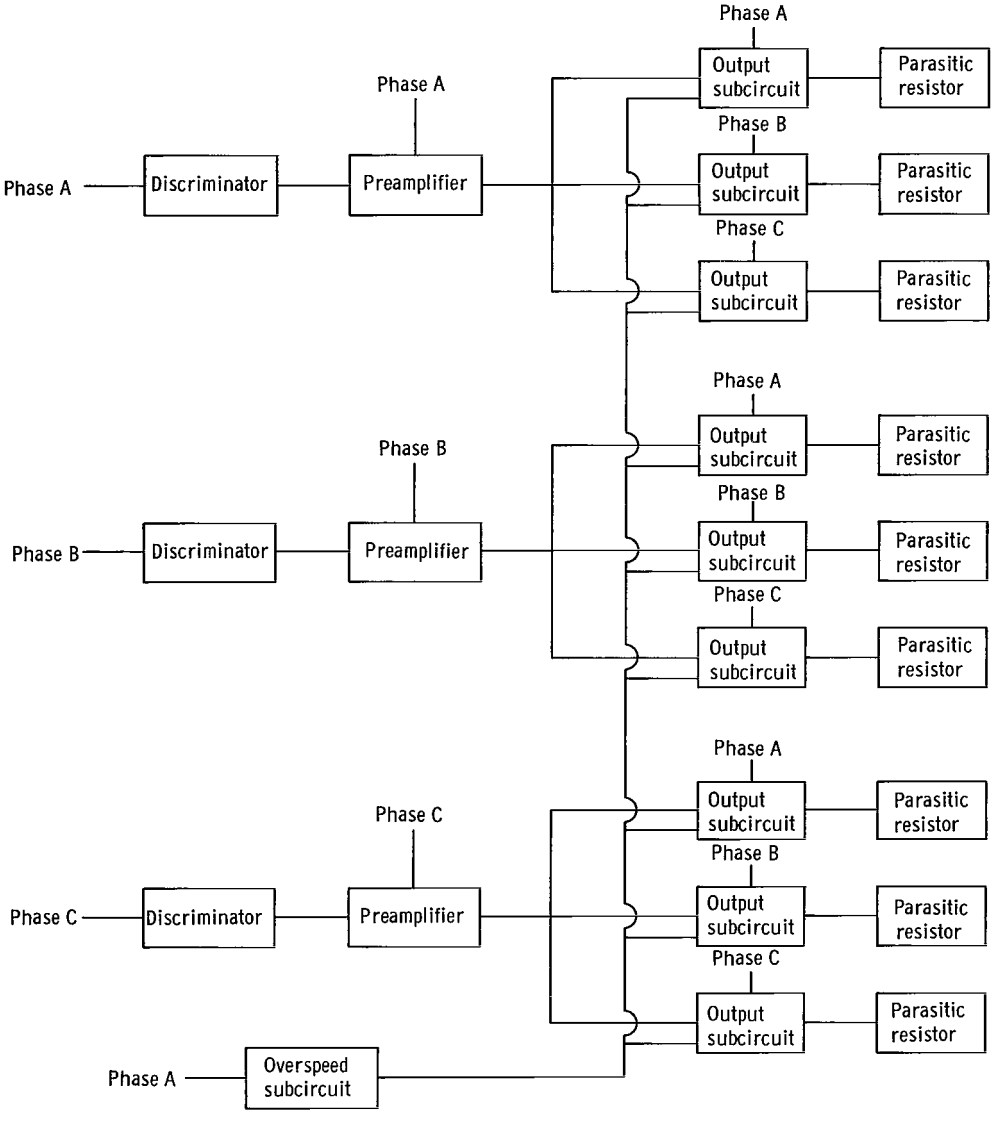



Figure 2. - Block diagram of speed controller.

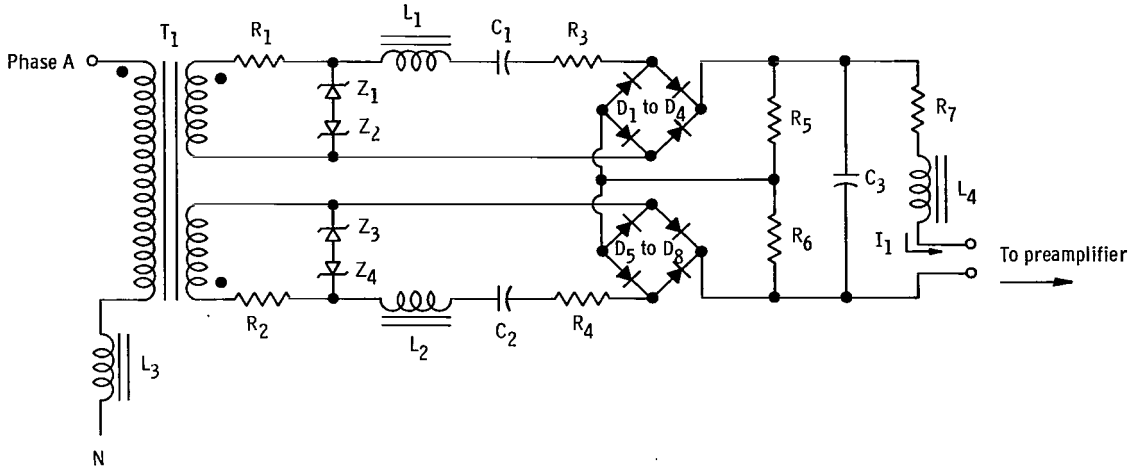



Figure 3. - Discriminator circuit diagram.

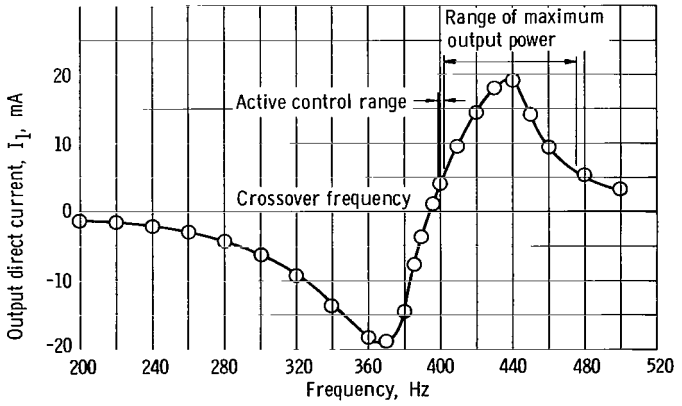



Figure 4. - Discriminator characteristic.

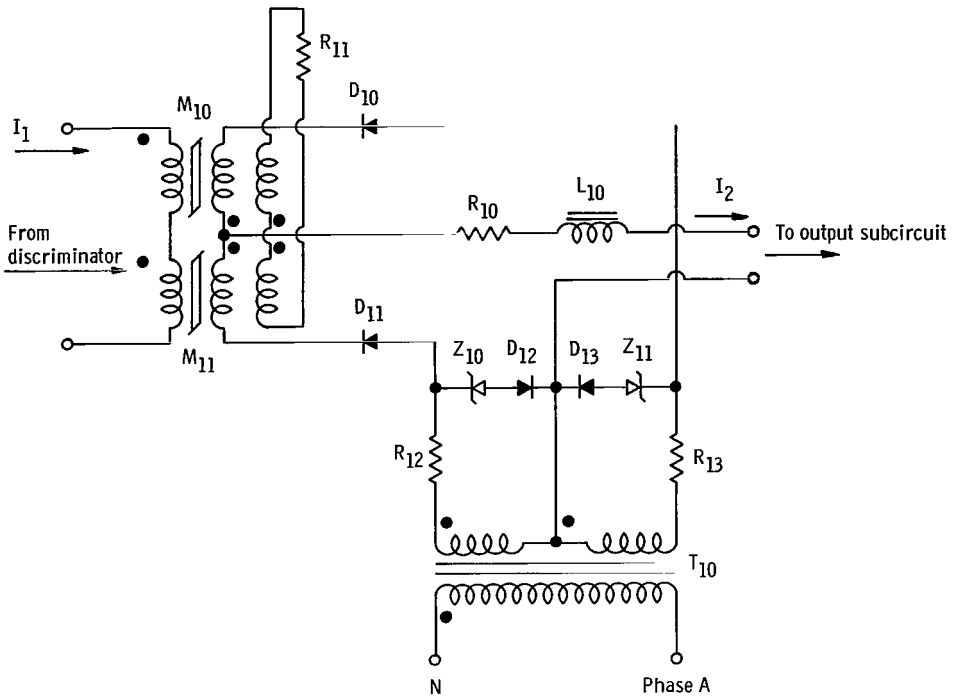



Figure 5. - Preamplifier circuit diagram.

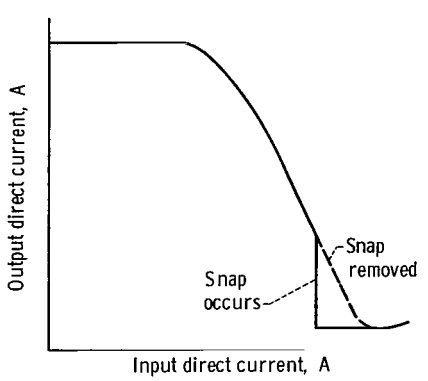



Figure 6. - Typical magnetic amplifier characteristic.

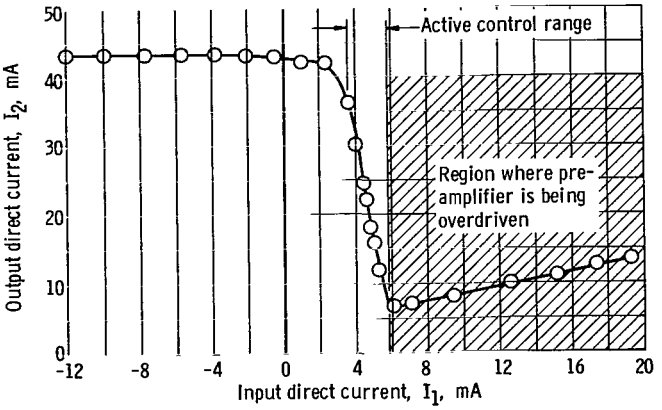



Figure 7. - Preamplifier characteristic.

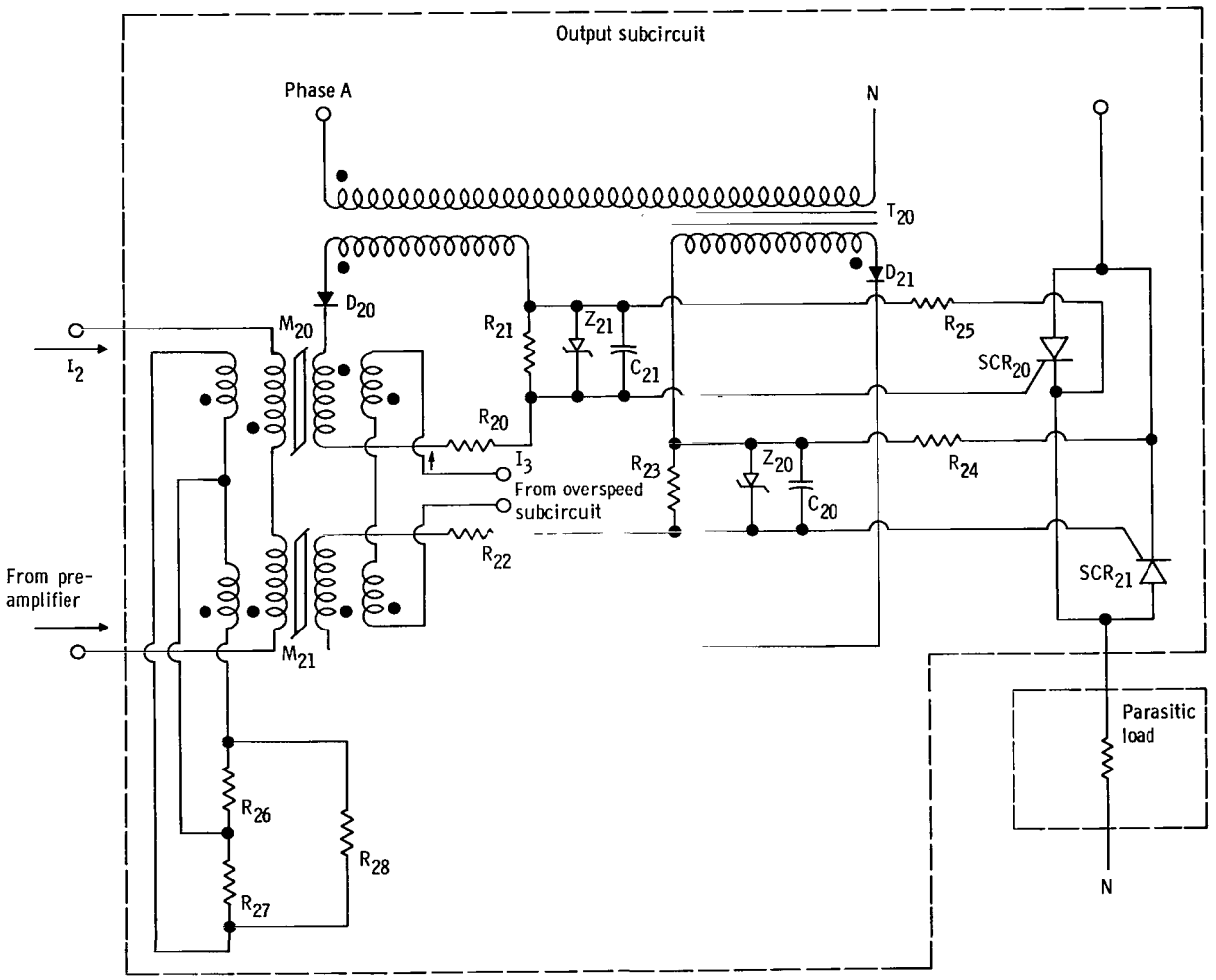



Figure 8. - Diagram of output subcircuit and parasitic resistor circuit.

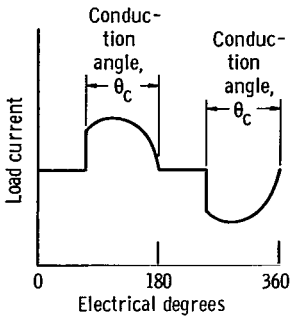



Figure 9. - Parasitic load current waveform.

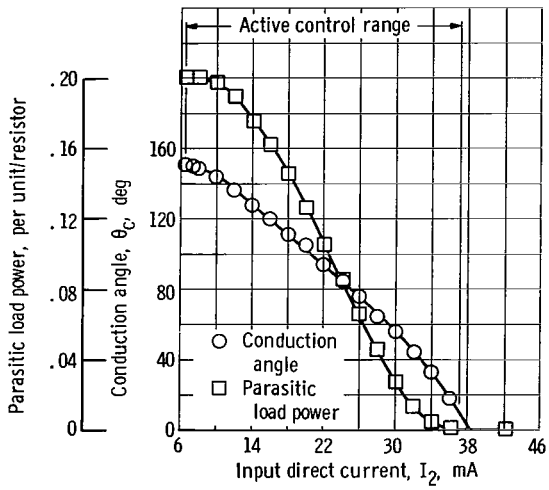



Figure 10. - Output subcircuit characteristic.

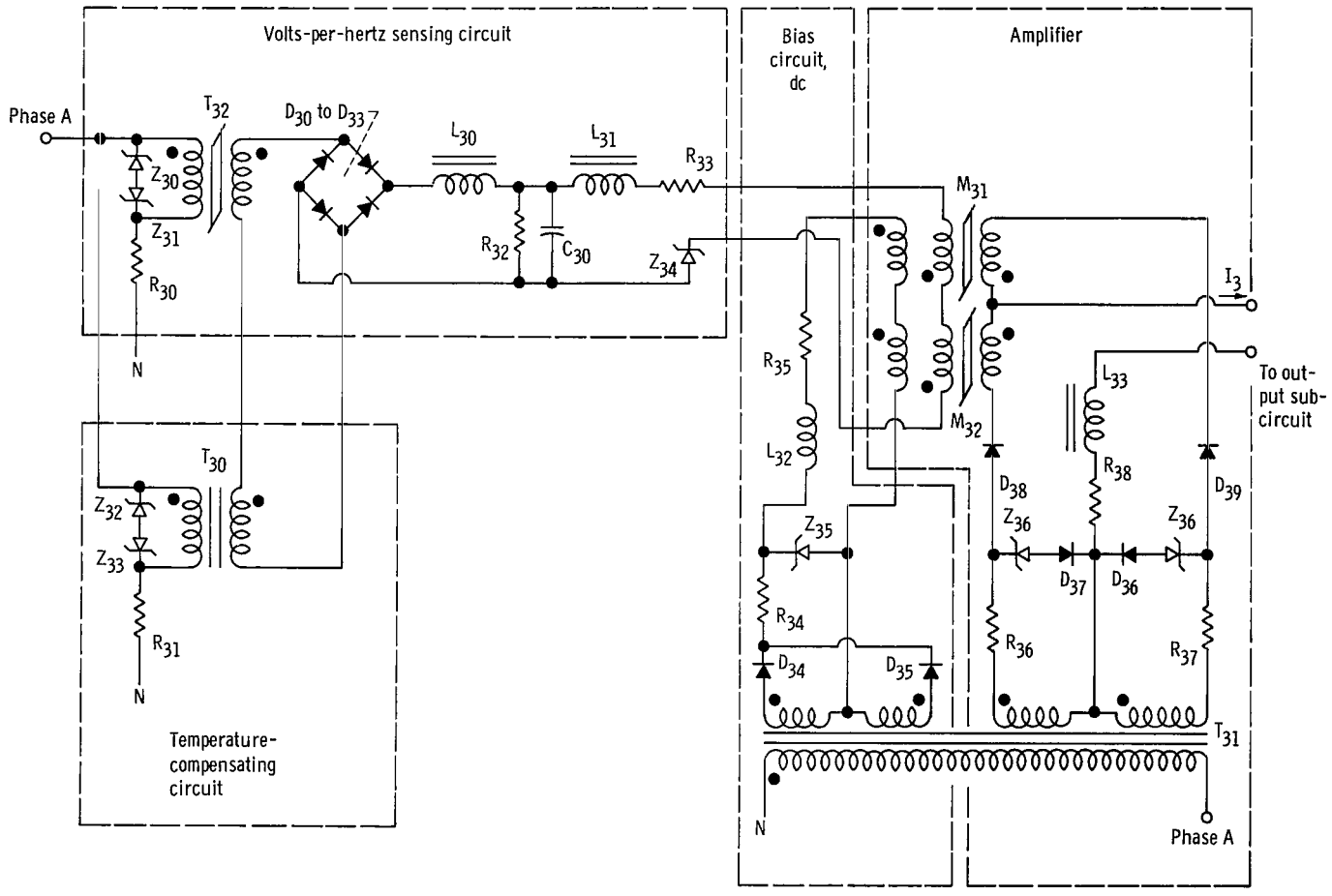



Figure 11. - Overspeed subcircuit diagram.

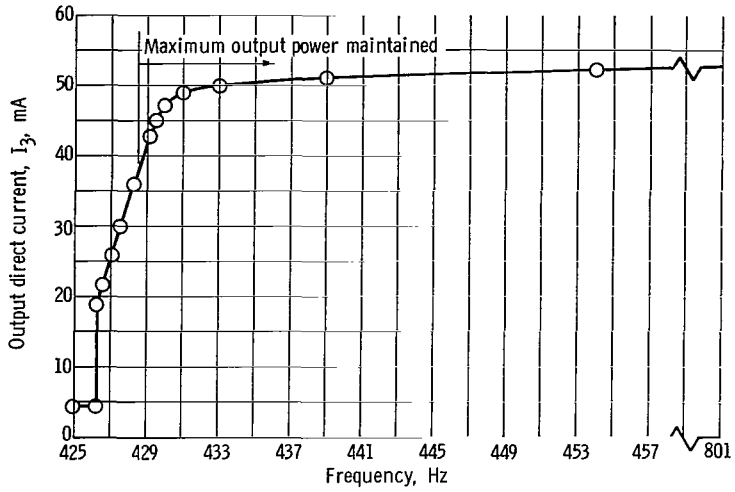



Figure 12. - Overspeed subcircuit characteristic.

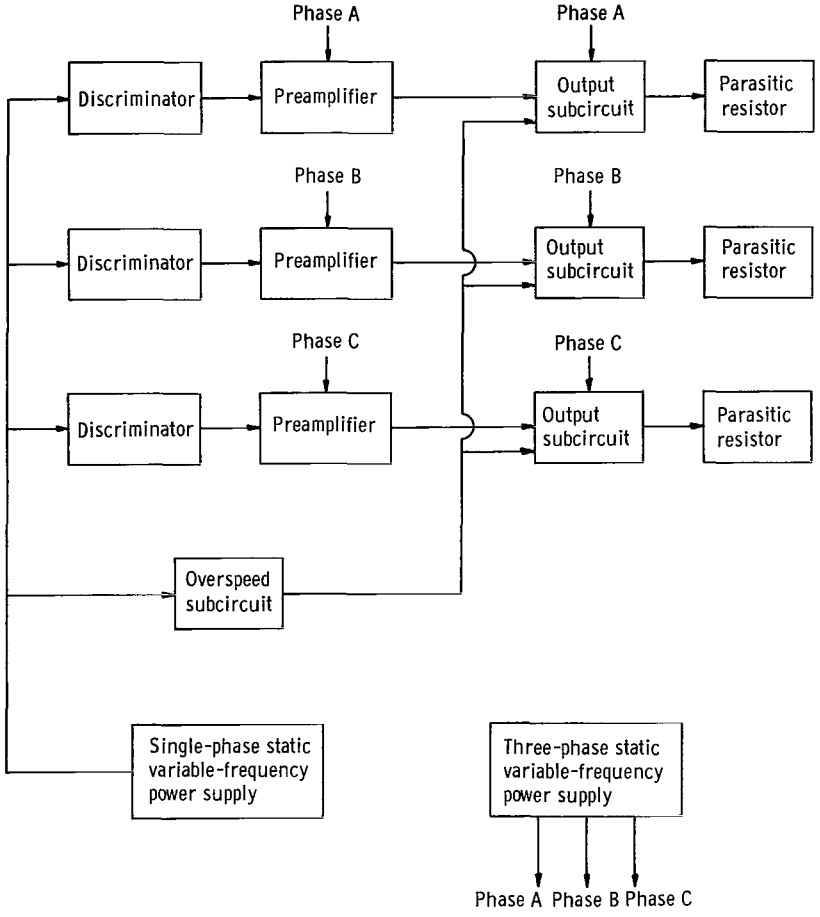
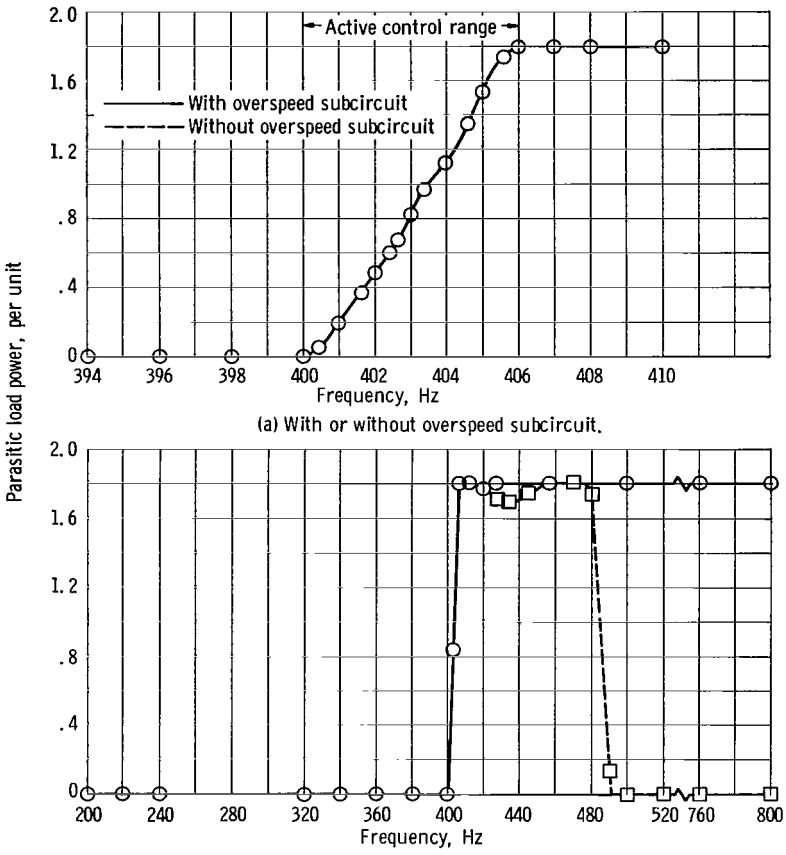



Figure 13. - Block diagram of experimental breadboard.




(a) With or without overspeed subcircuit.

(b) With and without overspeed subcircuit.

Figure 14. - Control characteristic of speed controller.